What is claimed is:

1. An apparatus comprising:

a hardware linked list, the hardware linked list including a plurality of nodes, each of the plurality of nodes including a next node pointer register; and

a locking mechanism to conditionally make the next node pointer register of each of the plurality of nodes read-only.

2. The apparatus of claim 1 wherein the locking mechanism comprises a control register.

3. The apparatus of claim 1 wherein each of the plurality of nodes includes a register operable to specify a capability of the apparatus.

4. The apparatus of claim 1 wherein the apparatus comprises a PCI local bus compliant peripheral device.

5. The apparatus of claim 1 wherein the apparatus comprises an integrated circuit having a microprocessor bus compatible interface.

6. A PCI local bus compliant device comprising:

a hardware implemented capabilities list capable of being modified by low-level software, and read-only to higher level software.

7. The PCI local bus compliant device of claim 6 wherein:

the hardware implemented capabilities list comprises a plurality of list nodes that each include a writeable next node pointer register.

8. The PCI local bus compliant device of claim 7 further comprising a control register coupled to the writeable next node pointer registers, the control register being operable to change the writeable next node pointer registers to read-only next node pointer registers.

9. The PCI local bus compliant device of claim 6 wherein the hardware implemented capabilities list is writeable by basic input output software and read-only to operating system software.

10. The PCI local bus compliant device of claim 6 wherein the PCI local bus compliant device comprises an integrated circuit that includes the hardware implemented capabilities list.

11. An integrated circuit comprising:

an address bus;

a data bus;

a control bus;

a series of linked list registers coupled to the address, data, and control busses, the series of linked list registers arranged in a writeable linked list; and

a control register operable to lock the writeable linked list and conditionally make the series of linked list registers read-only.

12. The integrated circuit of claim 11 wherein the series of linked list registers are arranged in groups, each group forming a linked list node, each linked list node including one next node pointer register.

13. The integrated circuit of claim 12 wherein the control register is operable to make the next node pointer register of each linked list node read-only.

14. The integrated circuit of claim 11 wherein the control register is accessible by a first level of software and the series of linked list registers are accessible by a second level of software, wherein the first level of software is lower than the second level of software.

15. The integrated circuit of claim 11 wherein the integrated circuit comprises a PCI local bus compliant computer peripheral.

16. An integrated circuit comprising:

a plurality of linked lists formed from registers;

a head pointer register to point to one of the plurality of linked lists; and

a control register to conditionally make the head pointer register read-only.

17. The integrated circuit of claim 16 wherein the control register is a write-once register.

18. The integrated circuit of claim 16 wherein each of the plurality of linked lists is formed from linked list nodes, each linked list node includes a writeable next node pointer register.

19. The integrated circuit of claim 18 wherein the control register conditionally makes the writeable next node pointers read-only.

20. The integrated circuit of claim 16 wherein the control register is a write-once register.

21. The integrated circuit of claim 16 wherein the control register can be written only once between system resets.

22. An integrated circuit comprising:

a first writeable register to signify whether a capabilities list is enabled;

a second writeable register to point to a capabilities list; and

a write-once control register operable to make the first and second writeable registers read-only.

23. The integrated circuit of claim 22 wherein the control register can be written only once between system resets.

24. The integrated circuit of claim 22 further including a hardware linked list pointed to by the second writeable register, the hardware linked list including a plurality of nodes, each of the plurality of nodes comprising a writeable next node register.

25. The integrated circuit of claim 24 wherein the control register is operable to make the writeable next node registers read-only.

26. The integrated circuit of claim 22 further comprising a PCI local bus compliant interface.

27. An integrated circuit comprising:

a plurality of register groups, each register group including registers operable to indicate capabilities of the integrated circuit, and including a next group register to point to a next group; and

a control register operable to render the plurality of register groups read-only.

28. The integrated circuit of claim 27 wherein the plurality of register groups form a PCI local bus compliant capabilities list.

29. The integrated circuit of claim 27 wherein the control register is modifiable once by basic input output software, and is not modifiable by operating system software.

30. The integrated circuit of claim 27 wherein the control register comprises a write-once lock bit, that when written, renders the plurality of register groups read-only.

31. The integrated circuit of claim 30 wherein the write-once lock bit is configured such that the write-once lock bit can be written to only once between hardware reset sequences.

32. A computer system comprising:

a bus;

a memory device with basic input output software coupled to the bus;

a peripheral device coupled to the bus, the peripheral device including a capabilities list implemented in groups of registers; and

a processor to execute instructions in the basic input output software to modify the capabilities list.

33. The computer system of claim 32 wherein the peripheral device further comprises a control register, that when written to, renders the groups of registers read-only.

34. The computer system of claim 33 wherein the memory device includes processor instructions stored therein to write to the control register.

35. The computer system of claim 32 wherein the peripheral device includes a PCI local bus compliant interface.

36. The computer system of claim 32 further comprising an add-in card upon which the peripheral device resides.

37. A computer system comprising:

a PCI local bus compliant peripheral device coupled to a bus; and

a processor coupled to the bus;

wherein the PCI local bus compliant peripheral device includes a capabilities linked list modifiable by the processor, and wherein the PCI local bus compliant peripheral device further includes a writeable control register operable to render the capabilities linked list read-only by the processor.

38. The computer system of claim 37 wherein the capabilities linked list comprises a plurality of nodes made up of groups of registers, each node corresponding to one capability and including one writeable next node pointer register.

39. The computer system of claim 38 wherein the writeable control register is operable to render the writeable next node pointer registers read-only.

40. The computer system of claim 37 further including a memory device having processor instructions stored therein, the processor instructions being operable to cause the processor to write to the writeable control register.

41. The computer system of claim 37 wherein the PCI local bus compliant peripheral device includes a writeable register to indicate whether the capabilities linked list is enabled.

42. A hardware linked list comprising:

a control register;

a first list node having a capabilities register and a next node pointer register; and

a second list node having a capabilities register and a next node pointer register;

wherein the next node pointer registers of the first and second list nodes are conditionally read-only in response to the control register.

43. The hardware linked list of claim 42 further comprising a writeable head pointer register to point to the first list node, the writeable head pointer register being conditionally read-only in response to the control register.

44. The hardware linked list of claim 43 wherein the hardware linked list is compliant with a PCI local bus rev. 2.2 capabilities list.

45. The hardware linked list of claim 42 wherein the control register is a write-once register.

46. The hardware linked list of claim 42 wherein the control register can be written to only once between hardware resets.

47. A method of initializing a computer peripheral comprising:

writing a list of capabilities to nodes in a hardware linked list within the computer peripheral; and

writing to a control register within the computer peripheral to make the nodes read-only.

48. The method of claim 47 wherein the nodes each include a capability register and a next node pointer register, and writing a list of capabilities comprises modifying the next node pointer register.

49. The method of claim 47 wherein writing to a control register comprises writing once to a capabilities lock bit, which thereafter is read-only.

50. The method of claim 47 further comprising writing to a capabilities list enabled register to signify whether the list of capabilities is enabled.

51. The method of claim 47 wherein the method is performed by basic input output software prior to loading of an operating system.

52. A method of initializing a PCI local bus compliant device comprising:

reading instructions from a memory device holding basic input output software;

modifying a link within a capabilities linked list in the PCI local bus compliant device; and

writing to a control register in the PCI local bus compliant device to make the link read-only.

53. The method of claim 52 wherein the capabilities linked list comprises a plurality of nodes, each node including a capabilities register and a next node pointer register, and wherein modifying a link comprises writing to the next node pointer register.

54. The method of claim 52 further comprising writing to a capabilities list enabled register.

55. The method of claim 52 further comprising writing to a head pointer register.

56. An apparatus having a computer readable medium with machine-readable instructions for a method stored thereon, the method comprising:

modifying a next node pointer register in a PCI local bus peripheral to indicate the existence of a capability; and

modifying a control register in the PCI local bus peripheral to make the next node pointer register read-only.

57. The apparatus of claim 56 wherein the method further comprises modifying a head pointer register to point to a hardware capabilities linked list, wherein the head pointer register becomes read-only responsive to the control register.

58. The apparatus of claim 56 wherein the apparatus comprises a read-only memory.

59. The apparatus of claim 56 wherein the method further comprises modifying a capabilities list enabled register, wherein the capabilities list enabled register becomes read-only responsive to the control register.